No. AN9329 September 1993

Application Note

Using the HI1176/HI1171 Evaluation Board

Introduction

The HI1176 (8-bit, 20MSPS, ADC) and the HI1171 (8-bit, 40MHz, DAC) evaluation board is composed of a main board common to either type, to which is added a sub board specific to each part. Each sub board is connected to the main board through a socket. The main board has an input interface, a clock buffer, and a latch.

Each of the sub boards is mounted with an HI1176 and HI1171 respectively.

Features

- **8-Bit Resolution**
- **20MHz Conversion Rate**
- **CMOS Digital Input Level**

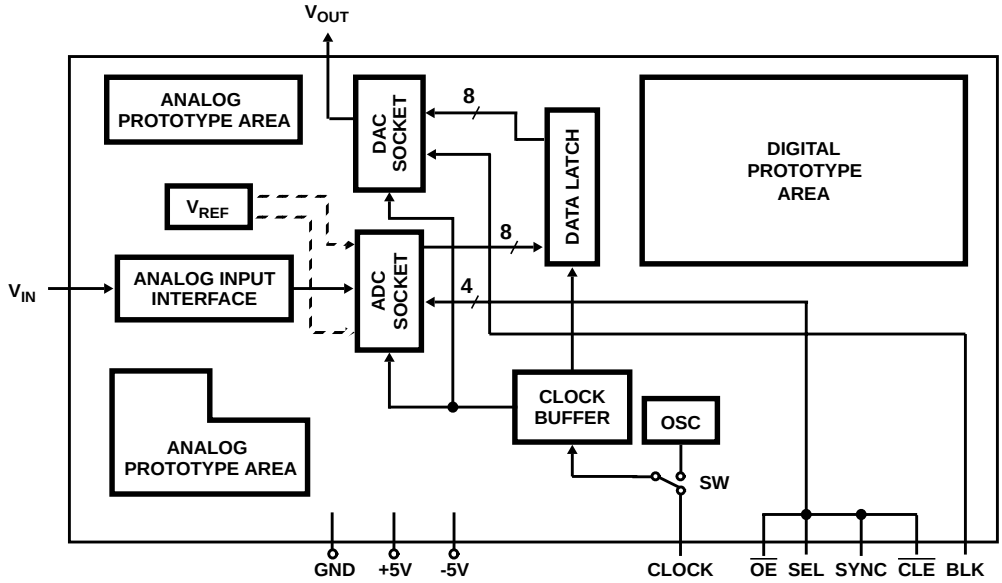
TABLE 1. SUPPLY VOLTAGE

ITEM	MIN	TYP	MAX	UNIT
+5V	-	-	150	mA
-5V	-	-	20	mA

TABLE 2. ANALOG OUTPUT (HI1171)

ITEM	MIN	TYP	MAX	UNIT
Analog Output	0.5	2.0	2.1	V

Functional Block Diagram



THE HI1176JCQ AND HI1171JCB ADC/DAC EVALUATION BOARD

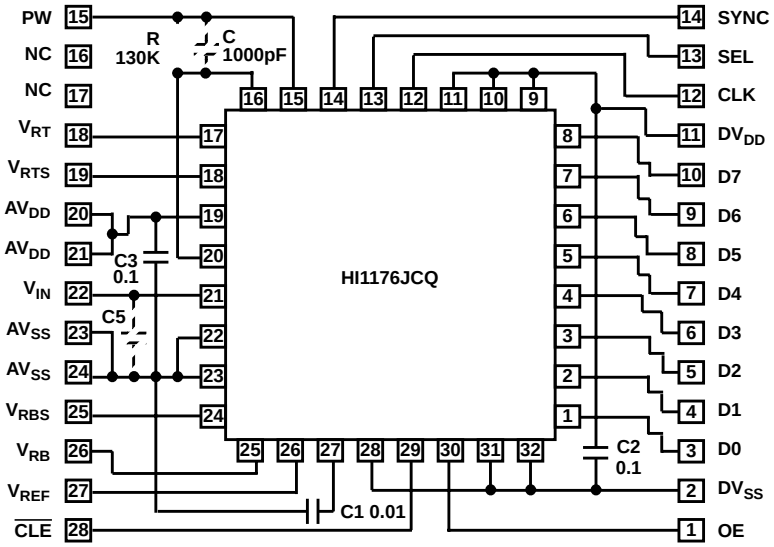
CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

TABLE 3. OUTPUT FORMAT (HI1176)

ANALOG INPUT VOLTAGE	STEP	DIGITAL OUTPUT CODE MSB								LSB
V_{RT}	0	1	1	1	1	1	1	1	1	
•	•									
•	•									
•	•									
•	127	1	0	0	0	0	0	0	0	
•										
•										

TABLE 3. OUTPUT FORMAT (HI1176) (Continued)

ANALOG INPUT VOLTAGE	STEP	DIGITAL OUTPUT CODE MSB								LSB
•	128	0	1	1	1	1	1	1	1	
•										
•										
•	•									
•	•									
•	•									
V_{RB}	255	0	0	0	0	0	0	0	0	



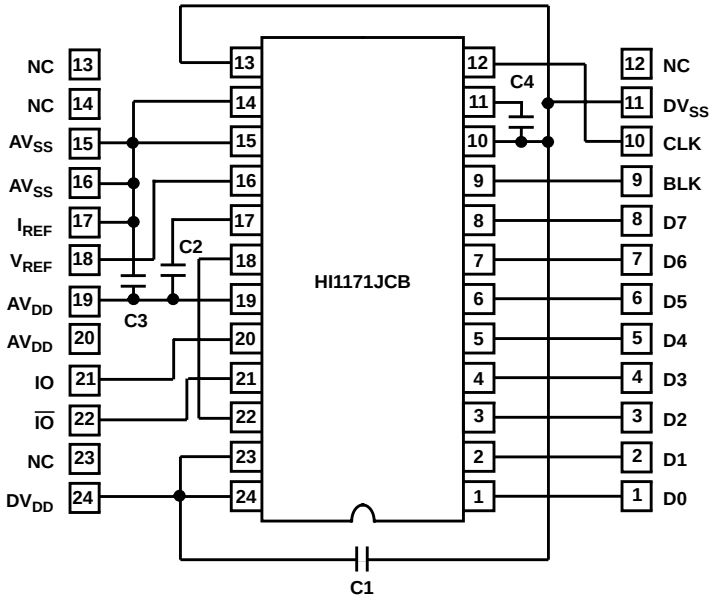


FIGURE 1. CMOS ADC/DAC PERIPHERAL CIRCUIT BOARDS
(Sub Boards)

Adjustment Method

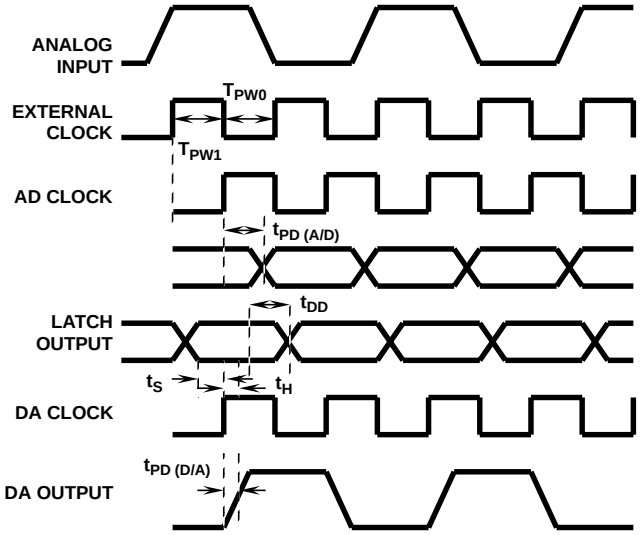
1. V_{REF} adjustment (VR1, VR2) - The A/D converter reference voltage. V_{RB} is adjusted by VR1 and V_{RT} is adjusted by VR2. When self bias is used, there is no need for adjustment. Reference voltage is set to self bias mode at delivery.
2. Clamp reference mode voltage adjustment (VR3) - Clamp reference voltage is set by VR3.
3. DAC output full scale adjustment (VR4) - Full scale voltage of the D/A converter output is adjusted to approximately 2.0V at shipment.
4. Sync (clamp) pulse interface (VR5) - This adjustment enables interface with the signal generator. At shipment, this adjustment is performed to obtain a threshold of approximately 2.5V to an H sync of 0V to 5V.
5. $\overline{OE}$, SEL, Sync, BLK, $\overline{CLE}$, Sync INT - The following pins are set on the main board: $\overline{OE}$, SEL, Sync, $\overline{CLE}$, Sync INT (HI1176) and BLK (HI1171). For the pins function, refer to the specifications. The difference between Sync pin and Sync INT pin is that you input a pulse above 3.5Vp-p to Sync INT pin. The pulse threshold is set through VR5. For input through Sync pin, pulse is input at TTL or CMOS level. In this case cut the line between the Sync pin and Sync INT pin.

   The PCB is shipped with the main board pins set as follows.

   - $\overline{OE}$ Low (A/D Output ON)
   - SEL Low (Pulse generated with Sync falling edge as trigger)
   - Sync Line junction with Sync INT pin
   - $\overline{CLE}$ Low (Clamp function ON)
   - BLK Low (Blanking OFF)
6. Clamp pulse input method - One method is to directly input the clamp pulse. Another method is to use the built-in multivibrator. The method used selected by using SW1. To use the built-in monostable multivibrator, it is necessary to mount the HI1176 sub board. R and C set the pulse width (ex. R = 130K, C = 100P, T_{PW} = 2.75µs).

TABLE 4. TIMING CHART

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Clock High Time	T_{PW1}	25	-	-	ns
Clock Low Time	T_{PW0}	25	-	-	ns
Clock Delay	T_{DC}	-	-	24	ns
Data Delay A/D	$t_{PD\ (A/D)}$	-	18	30	ns
Data Delay (Latch)	t_{DD}	-	-	17	ns
Setup Time	t_S	10	-	-	ns
Hold Time	t_H	2	-	-	ns
Data Delay D/A	$t_{PD\ (D/A)}$	-	10	-	ns

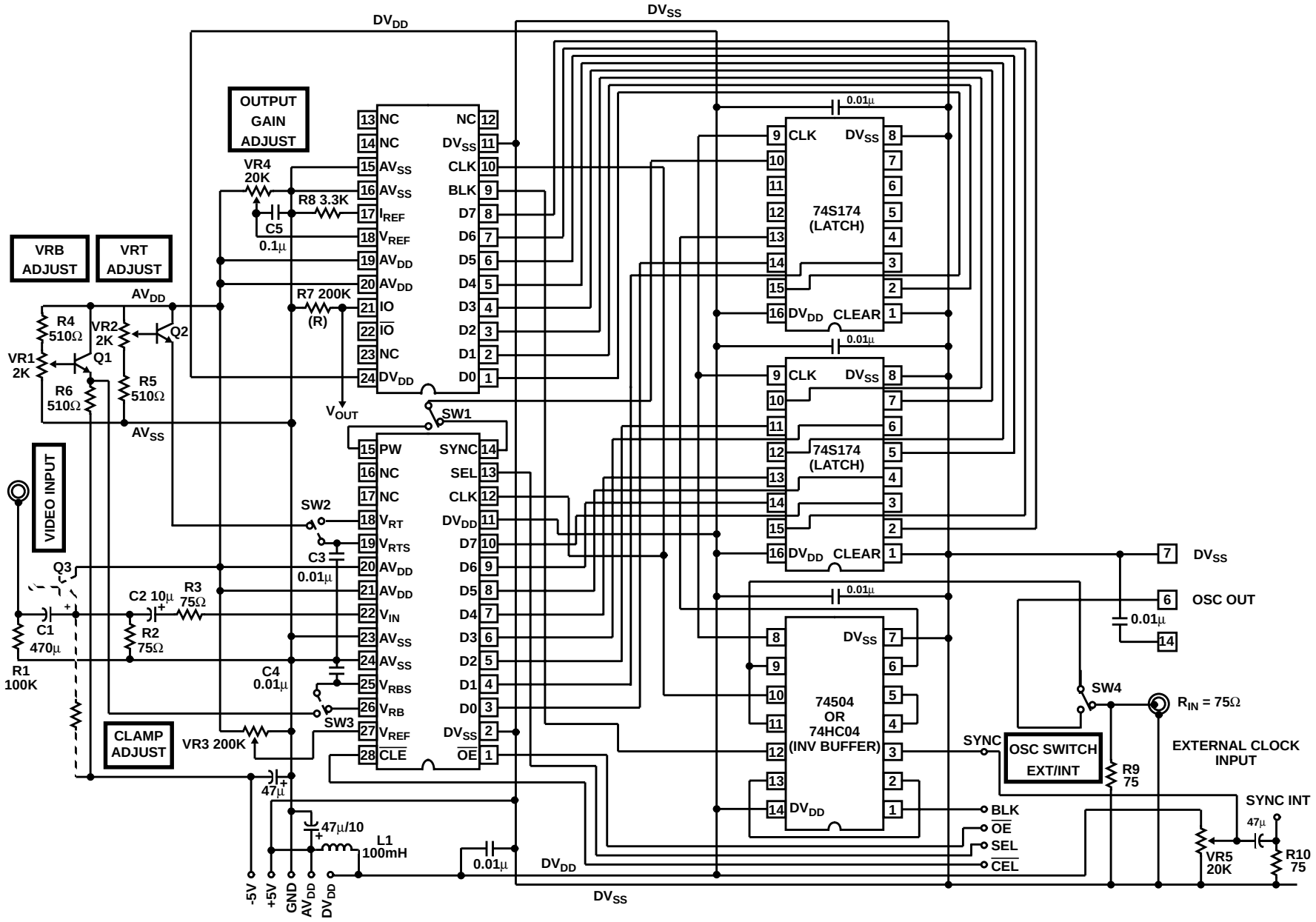


Notes on Operation

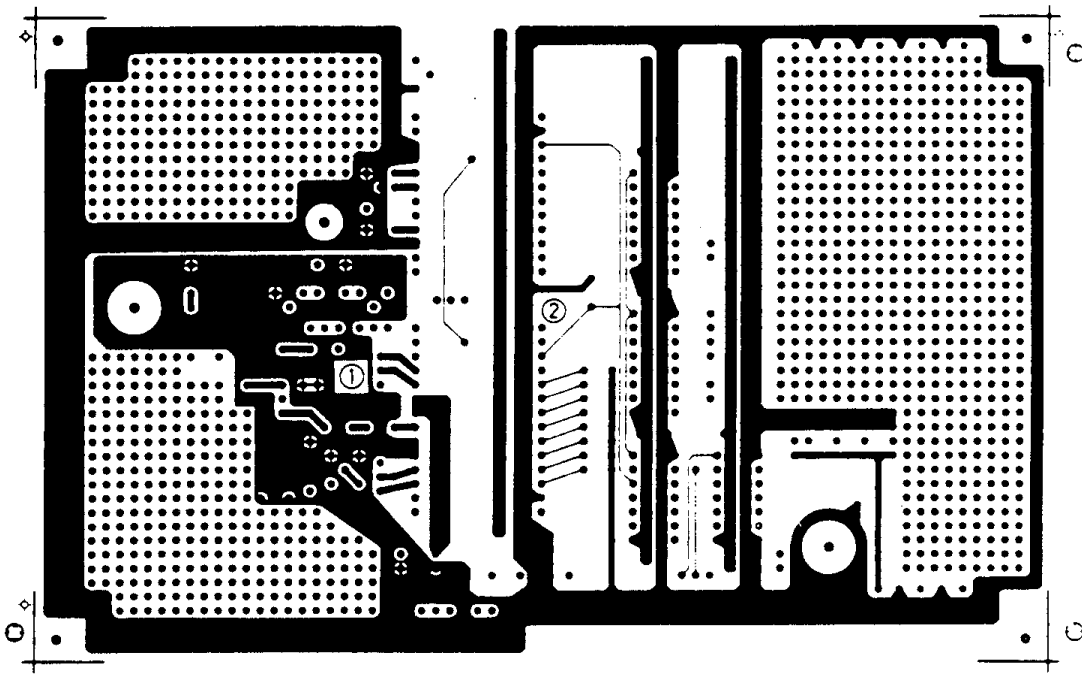
1. Reference voltage - Shorting V_{RT} and V_{RTS}, V_{RB} and V_{RBS} will activate the self bias function that generates V_{RT} = 2.6V and V_{RB} = 0.5V. On the evaluation board either self-bias or the external reference voltage can be selected depending on SW2 and SW3. At shipment from the factory, reference voltage is in self bias mode. To provide external reference voltage, adjust the dynamic range (V_{RT} - V_{RB}) to above $1.8V_{P-P}$.
2. Clock input - There are two modes for the evaluation board's clock input.

   1. provided from an external signal generator
   2. using the crystal oscillator (built-in clock driver).

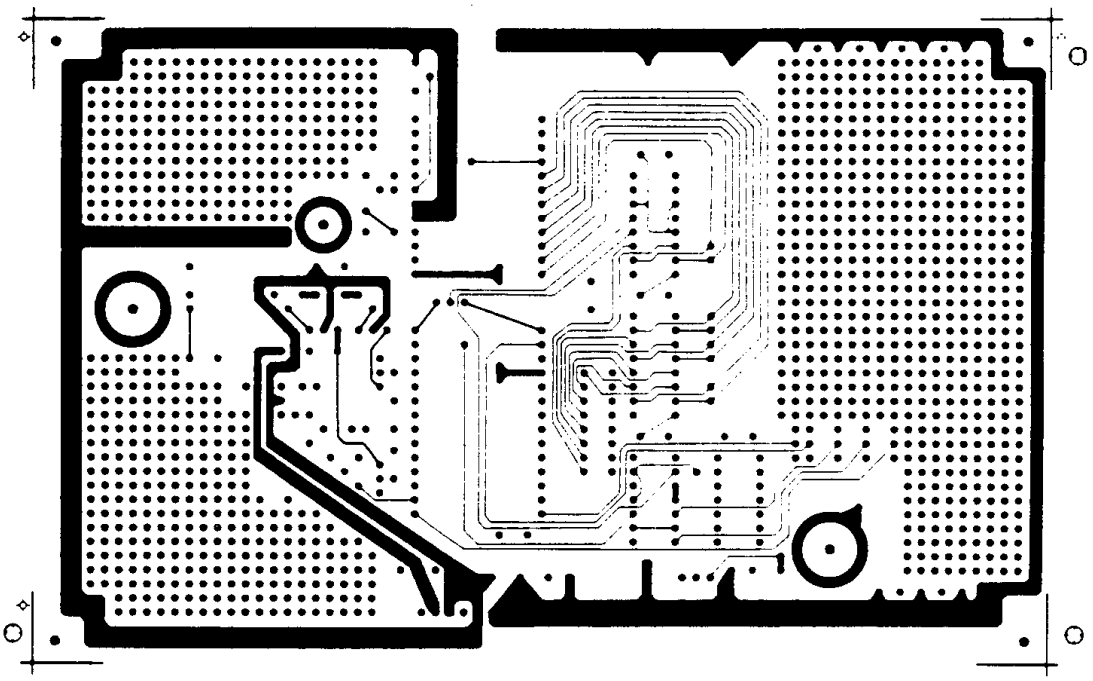
   One of the two modes is selected using the switch SW4 on the evaluation board.
3. The 2 latch ICs, 74S174, are not absolutely necessary for the evaluation of the ADC and the DAC. Operation will still be normal if the ADCs output is directly input to the DAC. However, since the ADCs output is usually converted by a DAC after some signal processing, the 74S174s were mounted to provide a signal processing example.
4. Setting CLE High will disable the clamp function. The DC portion of the input signal will be blocked by C2. The ADC side of C2 will settle to about $^1/_2$ (V_{RT} + V_{RB}). If it is desired to DC couple the input to the ADC, remove R2 and short C2. Q3 can also be used as a buffer.
5. Clamp pulse latch - On the evaluation board, the clamp is latched with the ADC sampling CLK and is then input to either the PW pin or Sync pin. A slight beat may be generated as vertical sag according to the relation between sampling frequency and clamp frequency. If there are no problems with V_{SAG}, latch is not necessary.
6. Prototype Areas - There is a group of throughholes on the analog input, output, and logic. These can be used when mounting additonal circuits on the evaluation board. The connector hole on the DAC board is used to mount the test chassis and the mount jack.


OUTPUT GAIN ADJUST
VRB ADJUST
VRT ADJUST
CLAMP ADJUST
VIDEO INPUT
VR4 20K
R8 3.3K
C5 0.1µ
R7 200K (R)
VR2 2K
R4 510Ω
VR1 2K
R6 510Ω
R5 510Ω
Q1
Q2
Q3
C1 470µ
R1 100K
C2 10µ
R3 75Ω
R2 75Ω
C3 0.01µ
C4 0.01µ
VR3 200K
47µ
47µ/10
L1 100mH
0.01µ
SW1
SW2
SW3
SW4
VOUT
AVDD
AVSS
DVDD
DVSS
-5V
+5V
GND
NC
AVSS
IREF
VREF
AVDD
IO
IO
DVDD
PW
SYNC
SEL
CLK
VRT
D7
VRTS
VIN
VRBS
VRB
CLE
D6
D5
D4
D3
D2
D1
D0
OE
BLK
74S174 (LATCH)
74504 OR 74HC04 (INV BUFFER)
CLEAR
OSC OUT
OSC SWITCH EXT/INT
RIN = 75Ω
EXTERNAL CLOCK INPUT
SYNC INT
R9 75
R10 75
VR5 20K

Evaluation Board



COMPONENT SIDE



SOLDER SIDE